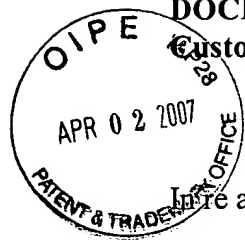DOCKET NO. 00-BN-051 (STMI01-00051) PATENT
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Anthony X. Jarvis, et al.

Serial No.: 09/751,372

Filed: December 29, 2000

For: SYSTEM AND METHOD FOR EXECUTING
VARIABLE LATENCY LOAD OPERATIONS IN A
DATA PROCESSOR

Group No.: 2183

Examiner: Aimee J. Li

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal. The review is requested for the reason(s) stated in the arguments below, demonstrating the clear legal and factual deficiency of the rejections of some or all claims.

The Office Action rejects Claims 1-22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,761,469 to *Greenley et al.* ("Greenley") in view of U.S. Patent No. 5,706,481 to *Hannah, et al.* ("Hannah"). For the convenience of the Panel, claim 1 describes:

1. (Previously Presented) A data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of

a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline;

a data cache capable of storing data values used by said pending instruction;

a plurality of registers capable of receiving said data values from said data cache;

a load store unit capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation;

a shifter circuit associated with said load store unit capable of one of a) shifting, b) sign extending, or c) zero extending said first data value prior to loading said first data value into said target register; and

bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit.

Claims 1, 14, and 23 recite a "load store unit" capable of transferring a first data value from a "data cache" to a "target one of [a] plurality of registers" during execution of a load operation. Claims 1 and 14 also recite a "shifter circuit" capable of shifting, sign extending, or zero extending the first data value "prior to loading [the] first data value into [the] target register." In addition, Claims 1 and 14 recite "bypass circuitry" capable of "transferring [the] first data value from [the] data cache directly to [the] target register without processing [the] first data value in [the] shifter circuit."

Claims 1, 14, and 23 are crystal clear – the "shifter circuit" can process a data value before the data value is loaded from a data cache into a target register. Also, the "bypass circuitry" can transfer the data value from the data cache directly to the target register without the data value being processed by the "shifter circuit" (thereby bypassing the shifter circuit).

Examiner Li alleges that Greenley teaches a shifter circuit corresponding to the claims, and that Greenley's sign extension unit 160 and alignment unit 170 together form the claimed "shifter circuit." Examiner Li is correct in that sign extension unit 160 does perform sign extending, and the alignment unit 170 does perform zero filling and shifting. In fact, Greenley teaches that the alignment <u>must</u> be assured, and that alignment unit 170 assures that the appropriate bits of the half-words are in the appropriate bit positions. *See col. 2, lines 19-30.* In Greenley's system, that the "shifter circuit" of 160/170 <u>cannot</u> be bypassed, as those functions <u>must</u> be present. The Examiner's response that the shifter circuit can be bypassed if there is "data that is already aligned, perhaps due to coincidence" is contrary to Greenley's express teachings, and illustrates the legal and factual deficiency of the rejection.

Greenley does not, and cannot, include "bypass circuitry" as claimed, and Greenley fails to disclose, teach, or suggest a structure that allows a data value to be transferred either (i) from a data cache to a target register through a shifter circuit, or (ii) directly from the data cache to the target register while bypassing the shifter circuit, as conceded in the Office Action.

Examiner Li alleges that "Hannah has taught bypassing functions circuitry capable of transferring said first data value to said target without processing said first data value in said shifter circuit." Examiner Li is incorrect -- no data cache is shown or described here, as required by the claims, and as Examiner Li attempts to ignore by simply referencing a "target". One cache described by Hannah is read cache 208, shown in Figure 2, which contains mip maps used by interpolator 209. Interpolator 209 resamples the texture image to produce the output samples, which are sent to the graphics rasterizer. These mip maps are not data values used by the pending instructions in an instruction execution pipeline, to transfer into a target register, as required by the claims. Nor do the TRAM caches meet the limitations of the claims, nor the I/O caches (*e.g.* 407).

Hannah does not teach or suggest bypass circuitry, as claimed, that is capable of transferring a first data value directly to a target register, as no registers are shown or described here. Hanna does not include any bypass circuitry that transfers any data values from a data cache to a register. Hannah does not teach or suggest bypass circuitry, as claimed, that is capable of transferring the first

data value without processing the first data value in a shifter circuit. Hannah does not teach or suggest bypass circuitry, as claimed, that is associated with a load store unit.

Examiner Li does not even attempt to show where these limitations may be found within Hannah or these figures, and fails to allege even a single specific element that could meet the claim limitations, a clear legal deficiency of the rejections. Examiner Li acknowledges that Hannah doesn't actually teach any bypass circuitry, stating instead that Hannah "suggests" that the multiplexers can be used to bypass certain capabilities. This is not a teaching of the claimed bypass circuitry, a specific hardware limitation, and illustrates that the rejections are legally and factually deficient.

Neither Greenly or Hannah, alone or in combination, teach or suggest doing anything in response to a determination that a pending instruction is a load word operation as recited in Claim 10. Examiner Li's rejection on this point repeats both the combination above and the motivation addressed below, neither of which teach or suggest anything at all with respect to this particular limitation, a clear legal deficiency.

Applicant further notes that the Examiner Li's stated motivation is that "bypasses improve the performance of a system by minimizing delays from unnecessary functions (Hannah column 9, lines 38-44)". This portion of Hannah is part of the passage reproduced above, and it is clear that there is no such teaching in this passage. While Hannah teaches a trade-off between precision/resolution and speed/cost, this has nothing to do with any bypass circuitry, despite the Examiner's rhetorical bootstrapping. There is no proper motivation in the reference itself, explicitly or implicitly, nor in the knowledge of one of ordinary skill in the art, nor in the problem to be solved.

CONCLUSION

As a result of the foregoing, the Applicant asserts that the claims in the Application are in condition for allowance over all art of record, and that the rejections are both factually and legally deficient, and respectfully requests this case be returned to the Examiner for allowance or, alternatively, further examination.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Munck Butrus Deposit Account No. 50-0208.

Respectfully submitted,

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